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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/653,958	05/22/96	PONTAROLLO	S S1022/7556

EXAMINER

E1M1/0220

LEJA,R

ART UNIT	PAPER NUMBER
2104	5

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DATE MAILED: 02/20/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 5-22-96.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-26 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-26 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

* U.S. GPO: 1996-409-290/40029

1. The drawings are objected to because Figure 1 needs to be labelled as "Prior Art". Correction is required.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the specific diode connections of Claim 11 and the first transistor comprising an N-channel MOS transistor and the second transistor comprising a P-channel MOS transistor of Claim 14 must be shown or the feature(s) cancelled from the claim(s). No new matter should be entered.

3. Claims 18-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is a lack of antecedent basis for "said first and second voltages" in lines 12 and 13 of Claim 18.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7, 12 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Pianka (5,345,357).

Pianka discloses (Fig. 2) a circuit comprising a first transistor (201) coupled to a first supply voltage (VDD) and a second supply voltage (VSS), a second transistor (204) coupled to a third terminal of the first transistor and a second terminal coupled to said second

supply voltage (via 202) and a capacitor (205) coupled between a third terminal of said second transistor and said first supply voltage (via 208, 209).

6. Claims 15 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Banura (5,023,542).

Banura discloses (Fig. 4) a device from protecting a circuit against surges wherein there is a first transistor (T3), a second transistor (T2), a third transistor (T1), a first power supply (+27v) and a second power supply (GND).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pianka.

Pianka discloses the use of a second resistor (206), but does not disclose the use of a first resistor being coupled between the third terminal of the first transistor and the first voltage supply. However, the use of the second resistor would have been obvious as a mere matter of engineering design choice. The second resistor, its connection between the gate and the first voltage supply and its value merely alter the biasing of the transistor and dismissing added space and cost requirements, would have been obvious to use so as to obtain the desired operating parameters of the circuit.

9. Claims 1-6, 8, 11, 13, 14 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pianka in view of Koepp (3,636,385).

These claims essentially add the limitations that the first transistor be of one type and the second transistor be of the second type, the use of a diode and specific connections with respect to the sources and the drains of the transistors. Pianka discloses that the first (201) and second (204) transistors are of the same type (n-channel), but that the protection circuit may be implemented utilizing (p-channel) MOSFETs and/or CMOS output buffers (i.e. 201-p, 202-n). Such changes would merely require such changes as reverse supply connections and etc...; the changes would be well within the abilities of one having ordinary skill in the art (col. 2, lines 29-68 and col. 5, lines 12-36). Koepp teaches (Fig. 1) a device for protecting a circuit wherein it is known to use a first transistor of a first type (16 p-channel), a second transistor of a second type (36 n-channel) coupled between the third terminal of the first transistor and a second supply (28) and the use of a diode (56). It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teachings Koepp and the disclosure of Pianka, as a matter of engineering design choice, in order to offer protection from any number of transient conditions, positive and negative, occurring at any supply terminal, while meeting the biasing and operating parameters of the circuit application, such as the voltage levels for transistor conduction and non-conduction thereby resulting in a highly reliable end-product.

10. Claims 16, 17, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banura in view of Merrill (5,239,440).

These claims essentially require that the third terminal of the third transistor be coupled to the first power supply through a capacitor and that the transistors are NPN bipolar transistors. Banura discloses the use of both NPN and PNP type bipolar transistors and the use of one type over the other would have been obvious as a mere matter of engineering design choice and well within the abilities of one having ordinary skill. These choices depend merely upon such considerations as whether one uses a negative or positive power supply for operation of the remaining circuitry. As to the use of a capacitor, Banura discloses the use of a sensing resistor for triggering, but Merrill teaches in Figures 1 & 5 and col. 4, lines 49-68), that a capacitor (36 or 47) in conjunction with a resistance may be utilized in the triggering of the protective feature composed of transistors. As such, it is the position of the examiner that it would have been obvious to one having ordinary skill in the art to incorporate the teachings of Merrill in that the use of a capacitor for triggering purposes would lend to a less power dissipating design during normal circuit operation while offering responsive triggering during spike conditions.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Ronald W. Leja whose telephone number is (703)308-2008.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)308-1782. The Group FAX numbers are (703)305-3431 or (703)305-3432.

RWL
RWL
February 17, 1997

Ronald W. Leja

RONALD W. LEJA
PATENT EXAMINER
GROUP 2100